

# Ilia A. Lebedev

Undergraduate Student  
Electrical Engineering and Computer Science  
University of California, Berkeley

*ilial@berkeley.edu*

[redacted for on-line publication]

---

**Objective** I seek to contribute to the field of computer science through research in the area of large-scale systems design, particularly many-core computer architectures. My main interest is the use of programmable logic devices as tools for rapid prototyping to aid the design space exploration of future architectures, but I am also interested in the hardware-software interface, reconfigurable computing, and VLSI systems design. In the long term, I intend to pursue an academic career involving post doctoral research, and eventually a professorship.

**Education** *University of California, Berkeley:*  
B.S. candidate: *Electrical Engineering and Computer Science*  
*(expected graduation Spring 2010) (GPA: 3.7)*  
*Emphasis:*

- *Digital design, large-scale systems design, computer architecture, VLSI.*
- *Operating systems, systems programming, languages, compilers.*
- *Mathematics, statistics.*

**Research**

**OpenRCL** *Oct. 2009 – Present*  
*Adviser: John Wawrzynek – UC Berkeley*  
Designed and implemented a flexible and scalable hardware platform to enable research in the area of reconfigurable computing. This project is in preparation for publication.

**On-Chip Network Simulator** *Oct. 2009 – Present*  
*Adviser: John Wawrzynek, Krste Asanović, John Lazzaro – UC Berkeley*  
Developing a tool to predict performance, area (90nm CMOS), and power characteristics of hierarchical on-chip interconnects for many-core architectures. The tool enables rapid design space exploration of on-chip interconnect topologies, helps locate potential problems, and automatically generates tuned implementations of hierarchical on-chip networks.

**Platform Interconnect Network** *Mar. 2009 – Present*  
*Adviser: John Wawrzynek – UC Berkeley*  
Designing and characterizing a scalable low-latency network for the BEE3 platform to enable a rapid prototyping of large-scale systems. This project is currently used for a global climate simulator (*GreenFlash*) by Lawrence Berkeley National Laboratory, as well as a joint Systems Biology effort by UC Berkeley and Stanford University.

**BCM: Bayesian Computing Machine** *Mar. 2009 – Oct. 2009*  
*Adviser: John Wawrzynek – UC Berkeley*  
Designed and implemented a Bayesian computing machine capable of evaluating arbitrary probabilistic networks using reconfigurable computing. A publication documenting this project will appear in the proceedings of the Eighteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, February 21-23, 2010.

**RAMP- Research Accelerator for Multiple Processors** *Jan. 2008 – Sep. 2009*  
*Advisers: John Wawrzynek, Greg Gibeling – UC Berkeley*  
Led a group of undergraduates working on components of a large system. Conducted several research projects in the context of the larger RAMP effort. Contributed extensively to a reconfigurable hardware library (*GateLib*) currently used by a number of academic and industrial research projects.

**FLINT**

Aug. 2008 – Dec. 2008

Advisers: John Lazzaro, Greg Gibeling – UC Berkeley

Designed, implemented, and verified a flexible, latency-insensitive SPARC V8 CPU generator capable of producing highly optimized designs for the Xilinx® Virtex 5 architecture. This project featured an extensive debugging framework, which exposed the architected state and allowed a seamless integration of components implemented in FPGA hardware with software emulation for complete visibility.

**BEEKeeper**

May 2007 – Oct. 2008

Advisers: John Wawrzynek, Greg Gibeling – UC Berkeley

Produced a proof of concept design exploring a scalable high-speed configuration and debug interface for large clusters of Xilinx® FPGAs using standard 100Base-Tx Ethernet and custom hardware.

**Professional****Electronics Support Group**, University of California, Berkeley May 2008 - Sep. 2008

- Evaluated candidate FPGA platforms for CS150 and other courses.
- Re-designed portions of infrastructure for a digital design course (CS150).
- Software, RTL, and PCB-level design.

**Software Engineer**, Access Softek, Inc Berkeley, CA June 2005 - Sep. 2007

- Developed, verified, and supported a commercial product.

**Teaching Experience****Head GSI (CS150)**, University of California, Berkeley Aug. 2008 – Jun.2009

- Helped shape the curriculum to modernize the digital design course.
- Delivered lectures, led recitation sections, and administered labs.
- Worked closely with the instructor of record.
- Outstanding teaching reviews: 4.90/5.00 average, 5.00/5.00 most current.

**Publications Posters and Talks****Academic Publications**

- M. Lin, I. Lebedev, and J. Wawrzynek, "High-Throughput Bayesian Computing Machine with Reconfigurable Hardware," Proceedings of the Eighteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, February 21-23, 2010.
- (In Preparation) M. Lin, I. Lebedev, J. Wawrzynek, and J. Lazzaro, "OpenRCL: From Sea-of-Gates to Sea-of-Cores," to be submitted for review to the International Supercomputing Conference, May 31–June 3, 2010.
- (In Preparation) M. Lin, I. Lebedev, J. Wawrzynek, and J. Lazzaro, "OpenRCL: A Familiar Platform for Reconfigurable Computing," to be submitted for review to the International Conference on Field Programmable Logic and Applications, August 31-September 2, 2010.

**Posters and Invited Talks**

- Iliia Lebedev, Christopher Fletcher, Alex Williams, "FLINT: A Flexible, Latency-Insensitive SPARC Implementation." RAMP Winter 2009 retreat.
- Iliia Lebedev, "BEEKeeper: A Scalable Programming and Management Tool for the BEE." BWRC Summer 2008 retreat.
- Iliia Lebedev, Christopher Fletcher, "FLINT: Generating a Flexible CPU." Talk given as part of the UC Berkeley IEEE Research Speaker Series.

**Skills**

- Extensive experience with large-scale system design.
- Extensive experience developing high-performance software and hardware.
- Experience leading a group in a large project setting.
- Experience designing, developing, and supporting a commercial product.
- In-depth knowledge of FPGA architecture.

References, transcripts, publications, and other information available upon request.